

Giuseppe Di Guglielmo

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Biosketch

Giuseppe Di Guglielmo is a Principal Engineer at Fermilab, an Adjunct Associate Professor in the Department of Electrical and Computer Engineering at Northwestern University, and a Designated Academic Colleague with the Department of Computer Science at Columbia University. He specializes in system-level design and hardware acceleration for AI/ML. He is part of the Fermilab AI Program and of the Fermilab team contributing to the DOE Genesis Mission, advancing AI-accelerated co-design workflows for scientific microelectronics and instrumentation. He works with scientists to develop intelligent detectors for harsh environments with ultra-low latency requirements. His recent projects include designing radiation-resistant, ML-enriched chips for the Large Hadron Collider and integrating ML algorithms for quantum readout and control into hardware operating at cryogenic temperatures. Before joining Fermilab, he was an Associate Research Scientist at Columbia University in New York and a postdoc at the University of Tokyo. He holds a Ph.D. in Computer Science and has over 15 years of experience with high-level synthesis for ASIC and FPGA design. He actively contributes to open-source communities for AI/ML acceleration and SoC design. He is an IEEE Senior Member.



Education

- **Ph.D. in Computer Science**, University of Verona, Italy, 2009
On the Validation of Embedded Systems through Functional ATPG
- **Laurea degree in Computer Science**, *Summa Cum Laude*, University of Verona, Italy, 2005
Verifica funzionale dei dispositivi digitali mediante manipolazione di Macchine a Stati Finiti Estese
- **Classical Studies Diploma**, Liceo Ginnasio di Stato Scipione Maffei, Italy, 1998



Appointments

- **Designated Academic Colleague**, March 2026 - present
Department of Computer Science at Columbia University, USA
- **Principal Engineer**, September 2025 - present
Technology Directorate, Intelligent Microelectronics Systems Division, Fermilab, USA
- **Adjunct Associate Professor**, December 2022 - present
Department of Electrical and Computer Engineering at Northwestern University, USA
- **Senior ASIC Engineer**, July 2022 - August 2025
Emerging Technology Directorate, Microelectronics Division, Fermilab, USA
- **Associate Research Scientist in Computer Science**, October 2013 - June 2022

Columbia University in the City of New York, USA

- **Postdoctoral Research Scientist in Computer Science**, November 2012 - September 2013

Columbia University in the City of New York, USA

- **Postdoctoral Fellow**, March 2010 - March 2011

VLSI Design and Education Center (VDEC), University of Tokyo, Japan

- **Postdoctoral Fellow**, April 2009 - February 2010, April 2011 - October 2012

University of Verona, Department of Computer Science, Italy



Visiting Experiences

- **Visiting Scholar**, August 2009 - February 2010

Purdue University, School of Electrical and Computer Engineering, USA

- **Research Intern**, September 2007 - December 2007

Certess Inc. (now Synopsys), France

- **Visiting Student**, October 2006 - February 2007

Tallinn University of Technology, Department of Computer Engineering, Estonia



Fermilab Highlights

- **Principal Investigator** for the proposal “Designing Smart Detectors with an ML-to-Silicon Platform,” submitted to the DOE FOA “Hardware-Aware Artificial Intelligence for High Energy Physics” (LAB 24-3305). The proposal included 17 co-PIs across seven institutions (Fermilab, Purdue University, University of Illinois Chicago, Cornell University, The University of Chicago, University of Illinois Urbana-Champaign, Texas Tech University). Awarded seed-year funding (start date September 1, 2025).
- **Senior Personnel** coordinating co-design efforts for “VIAS: Vertically Integrated Artificial Intelligence for Sensing and High-Performance Computing,” awarded under the DOE FOA “Microelectronics Science Research Center Projects for Energy Efficiency and Extreme Environments” (LAB 24-3320). Four-year project (start date January 2025).
- **Group Lead** representing the Intelligent Microelectronics Systems Division in the Fermilab AI Program, which coordinates AI strategy and activities across the laboratory (July 2025).
- **Adjunct Associate Professor** in the Department of Electrical and Computer Engineering at Northwestern University (December 2022).
- **Lead of an industrial collaboration** with Siemens EDA to deliver Catapult AI NN (integration of the open-source hls4ml with Siemens Catapult HLS) to meet the stringent edge-AI constraints of particle-detector applications. The framework enables domain scientists and AI experts to generate ASIC-ready neural accelerators without ASIC design expertise and streamlines workflows for experienced hardware engineers. [Official Siemens EDA press release](#) (May 21, 2024).
- **Lead for the co-design efforts** in the Intelligent Microelectronics Systems Division (since 2022); several chips fabricated to date, with additional designs in progress:
 - Co-designed a radiation-tolerant, reconfigurable ML autoencoder in ASIC for LHC front-end data compression using QKeras, hls4ml, and Catapult HLS; reduced power by 50% and area by 80%, achieving 2× performance vs. reference (65 nm LP CMOS).

- Led the co-design of ML-on-sensor filtering for CMS Phase-2 pixel ROICs: integrated an HLS classifier with the analog front-end in the pixelated area (TSMC 28 nm) to perform BX-rate data reduction at 40 MHz; achieved 54.4–75.4% bandwidth savings at $< 1 \text{ W/cm}^2$ total power (analog $\sim 5 \mu\text{W/pixel}$, digital $\sim 1 \mu\text{W/pixel}$).
- Developed a GF 65 nm test chip (“SPROCKET”) for on-sensor data compression in X-ray ptychography; evaluated principal component analysis vs. autoencoder implementations and achieved up to $70\times$ at-source compression with $\sim 20\%$ pixel-area increase.
- Co-designed “CryoAI,” a GF 22 nm SoC for quantum readout at 4 K with an integrated ML accelerator for on-chip inference; silicon is under test (wirebonded prototypes).
- Leading co-design efforts toward future tapeouts of ML algorithms for data compression and featurization for LHC/CMS experiments. This work is part of *SmartPixels*, a collaboration of physicists, engineers, and ASIC designers developing next-generation AI-integrated detector systems.
- **Co-developer of hls4ml**, an open-source ML-to-hardware compiler that translates trained models into synthesizable RTL for FPGA/ASIC flows. Lead of the extension to Siemens Catapult HLS; hls4ml is used widely across universities, U.S. national labs, and industry for low-latency ML deployments.
- **Co-lead of a Fermilab-driven collaboration** delivering the first embedded-ML integration for superconducting-qubit readout on the Fermilab Quantum Instrumentation Control Kit (QICK); produced an end-to-end specification-to-bitstream workflow (96% single-shot fidelity at 32.25 ns latency, $< 16\%$ LUTs). The collaboration spanned Fermilab’s Technology Directorate, the Computational Science and AI Directorate, and Purdue University.
- **Mentor for Master’s and Ph.D. students** advancing co-design of machine-learning algorithms for high-energy physics and quantum readout/control; mentored 10+ students from Columbia University and Northwestern University since 2022.
- Co-authored **over 25 Fermilab-affiliated publications** (since 2022). Details are in the *Research Activities* section.
- Filed a **provisional patent** with Fermilab: “Systems and Methods of Recurrent Convolutional Neural Network (RCNN) Decoding of Surface Codes for Quantum Error Correction (QEC)” (February 2025).
- **Co-presenter of a tutorial** with Siemens EDA at the IEEE/ACM Design Automation Conference (DAC): *Even Higher-Level Synthesis: An Exploration of AI Hardware Accelerators Using hls4ml* (June 2025). The tutorial showed how HLS and the open-source hls4ml framework translate Python-trained neural networks into synthesizable specifications for FPGA/ASIC flows, enabling low-latency and power-efficient acceleration. Fermilab case studies on LHC trigger systems and SmartPixels illustrated the strict constraints faced by engineers in the Intelligent Microelectronics Systems Division.



Professional Activities

Research Projects

– Designing Smart Detectors with an ML-to-Silicon Platform

Institution and Period: Fermilab, September 2025 – August 2026

Program: Hardware-Aware Artificial Intelligence for High Energy Physics

Sponsor: Department of Energy (DOE)

Position: Lead Principal Investigator

Abstract: Future scientific advancements for high-energy physics (HEP) experiments require $10\times$ increases in data volume and precision that demand optimized use of experimental data and accelerator run time, necessitating innovative detector technology. This proposal outlines an R&D program to

develop *smart detectors*, focusing on a pixel sensor with on-chip AI, capable of delivering physics-aware data compression that yields $5 - 10\times$ reductions in data rate while maintaining equivalent physics reconstruction performance of an uncompressed readout. Our R&D program addresses several key technical challenges stemming from next-generation ultra-high granularity particle physics experiments that are needed to identify new physics amidst unprecedented particle densities and event rates provided by future accelerator facilities. Traditional readout methods exceed bandwidth and latency constraints for streaming readout by 1-2 orders of magnitude in data rate per readout link and many tens of microseconds, respectively, making high-quality real-time data reduction in trigger systems crucial to achieving physics analysis goals. To meet these needs, we will develop power-efficient ($< 1\text{ W/cm}^2$), radiation-hard (above 1 Grad) front-end electronics capable of intelligent signal processing (enable data reduction from 100 Gbps to $< 5\text{ Gbps}$). This involves designing novel AI that can be implemented on application-specific integrated circuits (ASICs), and developing the datasets to train those AI algorithms. Building on our preliminary findings in the *SmartPixels* consortium, which developed intelligent algorithms for pixel sensor data reduction, we will pursue two new main objectives: solidifying the physics case for and subsequent technical requirements on a *SmartPixels* chip as part of an HL-LHC detector trigger system, and the initial design steps of a *SmartPixels* demonstrator readout chip that may be tested in future test beam campaigns. Our approach will enhance the scientific potential of existing hardware and broaden participation in the HEP AI ecosystem. We will make our $O(3M)$ event training single-pixel-cluster datasets, and instructions for achieving the aforementioned data compression ratios, available to the community, fostering new applications and collaboration between physicists, AI experts, and engineers. Designing the *SmartPixels* demonstrator ASIC in tandem with a clear physics case will be a crucial step towards specifying and meeting functional requirements and ensuring operational robustness, and proving this technique for applications across HEP. Our R&D program will also serve as an ideal training ground for future leaders at the intersection of physics, chip design, and machine learning.

– **Vertically Integrated Artificial Intelligence for Sensing and High Performance Computing (VIAS)**

Institution and Period: Fermilab, January 2025 – December 2028

Program: Microelectronics Science Research Center Projects for Energy Efficiency and Extreme Environments

Sponsor: Department of Energy (DOE)

Position: Senior Personnel

Hypothesis: 3D heterogeneous integration (3D HI) will enable energy-efficient sensing and high-performance computing (HPC) by significantly increasing precision and processing capacity while minimizing power consumption. Sensor modules will benefit from high-density interconnects for enhancing resolution by $4\times$ to $16\times$. Hybrid electronic-photonic AI accelerators integrated with sensors will reduce processing times by $\geq 100\times$ to 25 ns, and increase data filtering efficiency from $\sim 60\%$ to 99%, while maintaining $\geq 99\%$ accuracy. For HPC systems, which need $100\times$ greater energy efficiency than current exascale machines, hybrid electronic-photonic AI accelerators with HBM will enable in-memory compute and efficient workload distribution across energy-efficient custom hybrid nodes, optimizing system performance and supporting distributed workloads to meet the power and performance needs of zettascale computing.

– **Adaptive Edge-ML Accelerators for Integrated Data Analysis and Discovery in HEP**

Institution and Period: Fermilab & Northwestern University, June 2023 – March 2026

Sponsor: Department of Energy

Position: Senior Personnel

Goals: The major goals of this project are to investigate efficient methods for achieving adaptiveness using the embedded FPGA (eFPGA) technology and create the necessary computing infrastructure to operate this technology efficiently. The proposed computer architecture and the accompanying design methodology will: (i) support post-deployment reconfiguration of the initial ML-edge hardware

guided by the scientists, as experiment data collected in the field prompts them to address the pre-deployment model dataset’s limitations as well as changing experiment conditions; and (ii) provide autonomous adaptation of the edge-ML hardware via training at the edge. The first step towards achieving the adaptiveness is to successfully integrate the eFPGA technology into our proposed heterogeneous system-on-chip (SoC) architecture for embedded systems. The next major technical goal is to create the newly integrated system including the eFPGA fabric as a physical artifact, which will then need to undergo testing, verification, and characterization to extract its practical operating parameters and performance specifications. Alongside this effort, the supporting design tools and the programming/reconfiguration environment for this new computing device will be developed. The supporting design environment will also require a pipeline for feeding data to satisfy the needs for adaptation, representing the dynamic behavior of the workload, i.e., the science application.

– **A Real-Time HPC Platform with In-Memory, Non-Von-Neumann Processing and Optical Networking (ARION)**

Institution and Period: Columbia University, January 2020 – June 2022

Program: Digital RF Battlespace Emulator (DRBE)

Sponsor: Defense Advanced Research Projects Agency (DARPA)

Position: Researcher

Abstract: The Digital RF Battlespace Emulator (DRBE) program aims to create the world’s first large-scale, virtual radio frequency (RF) environment for developing, training, and testing advanced RF systems, such as radar and electronic warfare (EW) systems. The target DRBE environment will enable numerous RF systems to interact with each other in a fully closed-loop RF arena, replicating dense, responsive, real-world RF environments. RF systems increasingly use artificial intelligence (AI) to help automate and augment capabilities for defense use. DRBE is exploring novel computing architectures to enable the creation of a new breed of High-Performance Computing (HPC) – dubbed “Real Time HPC”. The RT-HPC aims to generate computational performance in the double-digit petaFLOPs class while maintaining single-digit microsecond scale end-to-end latency.

– **Efficient Programmability of Cognitive Heterogeneous Systems (EPOCHS)**

Institution and Period: Columbia University, January 2018 – June 2022

Program: Domain-Specific System on Chip (DSSOC)

Sponsor: Defense Advanced Research Projects Agency (DARPA)

Position: Researcher

Abstract: The project goal is to develop a heterogeneous system-on-chip composed of many cores that mix general purpose processors, special purpose processors, hardware accelerators, memory, and input/output (I/O) devices to significantly improve the performance of domain-specific applications of interest for the Department of Defense (DoD). The project explores architectures that improve computing efficiency through specialized processing while maintaining programmability. Dr. Di Guglielmo’s research focuses on developing automation methods for the system-level design and optimization of accelerators specialized for machine learning applications.

– **Embedded Computing for Embodied Learning**

Institution and Period: Columbia University, July 2019 – June 2022

Sponsor: SEAS Interdisciplinary Research Seed (SIRS) at Columbia University

Position: Researcher

Abstract: The project aims to embed computational power in a highly distributed fashion inside a robot’s body. The traditional paradigm calls for data from the robot’s sensors to be centralized to one powerful computer, often sitting outside the robot’s body, to run learning algorithms that require high computing power. By distributing powerful, energy-efficient embedded computer platforms throughout the robot’s body, the robot can process sensor data right where it is harvested and use it to develop

new motor skills. The robots designed in this project move through debris and clutter in disaster response or search-and-rescue operations. Dr. Di Guglielmo focuses his research on robotic motor learning by leveraging embedded computing under power and computation constraints.

– **Acceleration of Deep Neural Networks via Heterogeneous Computing for Real-Time Processing of Neutrino and Particle Imagery**

Institution and Period: Columbia University, March 2018 – June 2022

Sponsor: Research Initiatives in Science & Engineering (RISE) at Columbia University

Position: Researcher

Abstract: The project aims to develop a system to facilitate real-time classification of images streamed at a massive scale, with the ultimate goal of leveraging recent advancements in computer science to accelerate particle physics discovery. The main application of the system is the upcoming Deep Underground Neutrino Experiment (DUNE). DUNE is a major international particle physics experiment aimed at continuously streaming high-resolution 3D images at over five terabytes per second. It was expected to commence in 2024 and to be operational for over a decade. Dr. Di Guglielmo's research focuses on designing a scalable computing system that employs machine learning and field-programmable gate arrays (FPGAs) to identify and classify interesting activity in the data. The ability to process this data in real time could enable the discovery of rare particle interactions which have never before been observed.

– **Rethinking CAD for System-Level Design via Interactivity, Learning, and Collaboration**

Institution and Period: Columbia University, June 2015 – June 2022

Sponsor: National Science Foundation, Software and Hardware Foundations (SHF)

Position: Researcher

Abstract: The core part of this project was developing a new senior-level undergraduate course unique in its use of a collaborative Computer-Aided Design (CAD) environment. Dr. Di Guglielmo developed a highly interactive CAD environment for System-Level Design to promote continuous collaboration across teams of students and inspire creative engineering solutions. The proposed approach leverages his work on compositional design-space exploration and machine learning to assist designers in using advanced synthesis tools.

– **Hardware-Up Security Antifragility and Automation**

Institution and Period: Columbia University, January 2018 – April 2019

Program: System Security Integrated Through Hardware and Firmware (SSITH)

Sponsor: Defense Advanced Research Projects Agency (DARPA)

Position: Researcher

Abstract: The SSITH program involved eight research institutes: Columbia University, MIT, Cornell, University of Michigan, University of California San Diego, Charles Stark Draper Laboratory, Lockheed Martin, and SRI International. The overall goal of SSITH was to develop “hardware design tools that provide security against hardware vulnerabilities that are exploited through software in Department of Defense and commercial electronic systems”. Dr. Di Guglielmo's research focused on defining security mechanisms between the hardware and software interfaces of modern Systems on Chip and hardware accelerators. The approach systematically strengthens each layer in the system stack, from the low-level hardware to the user-application software.

– **ESP: Embedded Scalable Platforms for Terascale Energy Efficient Computing**

Institution and Period: Columbia University, February 2012 – August 2017

Program: Power Efficiency Revolution for Embedded Computing Technologies (PERFECT)

Sponsor: Defense Advanced Research Projects Agency (DARPA)

Position: Researcher

Abstract: Dr. Di Guglielmo was a lead designer in this project, which was part of the DARPA multi-year program Power Efficiency Revolution for Embedded Computing Technologies (PERFECT) that started in February 2012 and completed its goals in August 2017. The PERFECT program aimed to research and develop the technologies to provide the power efficiency required by future military systems. The goal of ESP was to create a novel design methodology for digital integrated circuits that improves the amount of computation performed per watt.

– **Center for Future Architectures Research (C-FAR)**

Institution and Period: Columbia University, January 2013 – December 2017

Sponsor: Semiconductor Research Corporation (SRC) & Defense Advanced Research Projects Agency (DARPA)

Position: Researcher

Abstract: Semiconductor Research Corporation (SRC) & Defense Advanced Research Projects Agency (DARPA) founded the C-FAR project. The research center was focused on creating the future generation of scalable computing systems and completed its goals in December 2017. It accomplished its goals through a highly collaborative research agenda that brought together researchers from many top-tier universities, including Columbia, Duke, Harvard, MIT, Princeton, Stanford, UC Berkeley, and the University of Michigan. Dr. Di Guglielmo's research focused on improving the speed, throughput, and efficiency of the computation of heterogeneous, customized, and application-specific architectures.

– **A CORRECT-by-CONSTRUCtION Workbench for Design and Verification of Embedded Systems (COCONUT)**

Institution and Period: University of Verona, January 2008 – June 2010

Sponsor: European Union Project FP7-ICT

Position: Research student, then Postdoctoral Fellow

Abstract: The COCONUT project's aim was to define a formal framework based on tight integration of design and verification through all the refinement steps of an embedded platform design flow, from the specifications to the logic synthesis and software compilation. The project proposed a modeling and verification flow to enhance and speed up the embedded platform design and configuration. The project also designed mixed continuous and discrete models for managing multimedia and sensor networks.

– **Verification and Validation of Embedded System Design Workbench (VERTIGO)**

Institution and Period: University of Verona, June 2006 – November 2008

Sponsor: European Union Project FP6-IST

Position: Research student

Abstract: The VERTIGO project aimed to develop technologies and tools to integrate the verification of embedded systems in configurable platforms within economic and technical constraints. VERTIGO leveraged the results and tools coming from the previous IST-FP5 SYMBAD project and widened the spectrum of formal techniques applied to the verification of embedded systems.

Services to the Technical Community

Over the years, Giuseppe Di Guglielmo has served as a reviewer and as a member of the Technical Program Committee (TPC) for numerous international journals and conferences. A partial list includes:

– **Member of Technical Program Committee**

- IEEE International Conference on Computer Design (ICCD), 2019
- IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC), 2014

- IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2014
- IEEE/CAS International Conference on VLSI Design (VLSID), 2014
- Haifa Verification Conference (HVC), 2013
- **Reviewer for International Journals**
 - *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*
 - *International Journal of Parallel Programming*
 - *IEEE Embedded Systems Letters (ESL)*
 - *Journal of Systems and Software (JSS)*
- **Reviewer for International Conferences and Workshops**
 - *IEEE/ACM Design Automation Conference (DAC)*
 - *ACM/IEEE Design, Automation and Test in Europe (DATE)*
 - *International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES)*
 - *International Conference on Embedded Software (EMSOFT)*
 - *ACM/IEEE International Conference on Formal Methods and Models for System Design (MEM-OCODE)*
 - *International Conference on Computer-Aided Design (ICCAD)*
 - *IEEE High Performance Extreme Computing Conference (HPEC)*
 - *IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)*
 - *International Test Conference (ITC)*
 - *ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED)*
 - *International Workshop on Logic and Synthesis (IWLS)*
 - *ACM International Conference on Computing Frontiers (CF)*
 - *IEEE International Parallel and Distributed Processing Symposium (IPDPS)*
 - *IEEE International Conference on Computer Design (ICCD)*
 - *Haifa Verification Conference*
 - *International Symposium on Games, Automata, Logics, and Formal Verification (GandALF)*



Research Activities

Giuseppe Di Guglielmo has authored and co-authored more than 100 publications, achieving an h-index of 30 (Google Scholar, [ResearchGate](#)). Selected publications are provided, including the Scimago h-index for each journal article and the sponsoring organization for each conference paper. Prestigious sponsors, including the Institute of Electrical and Electronics Engineers (IEEE) and the Association for Computing Machinery (ACM), have a long-standing tradition of endorsing and disseminating high-quality scientific research. Entries marked with  denote Fermilab affiliation.

Patents

- P1.  Ulascan Sarica, Giuseppe Di Guglielmo, Cheong Yiu Li, Gabriel Nathan Perdue, *Systems and Methods of Recurrent Convolutional Neural Network (RCNN) Decoding of Surface Codes for Quantum Error Correction (QEC)*, February 2025 (provisional, # 63/758,184)

Journal Publications

- J30. ✿ Jan-Frederik Schulte, Ho Fung Tsoi, Noah Paladino, Abhijith Gandrakota, Sioni Summers, Daniel Diaz, Javier Campos, Enrico Lupi, Philip Harris, Christian Herwig, Duc Hoang, Santosh Parajuli, Marco Colombo, Maurizio Pierini, Chang Sun, Benjamin Ramhorst, George A Constantinides, Stylianos Tzelepis, Seda Ogrenci, David Burnette, Russell Marroquin Solares, Haoyan Wang, Vladimir Lončar, Alexander Tapper, Ryan Forelli, Rian Brooks Flynn, Nhan Tran, Thea Klaeboe Aarrestad, Elham E Khoda, Dimitrios Danopoulos, Giuseppe Di Guglielmo, Javier Duarte, Scott Hauck, Zhiqiang Que, Nicolò Ghielmetti, Quentin Berthet, Mia Liu, Lino Gerlach, Jovan Mitrevski, Bo-Cheng Lai, Melissa Quinnan, Dylan Rankin, Ben Hawks, Lauri Laatu, Jennifer Ngadiuba, Mark S Neubauer, Farah Fahim, Paul White, Konstantinos Axiotis, Wayne Luk, Suleyman Demirsoy, Shih-Chieh Hsu, Manuel Valentin, *hls4ml: A Flexible, Open-Source Platform for Deep Learning Acceleration on Reconfigurable Hardware*, ACM Transactions on Reconfigurable Technology and Systems, Vol. 19, No. 2, 2026, pp. 1-35, h-index 38
- J29. ✿ Benjamin Hawks, Giuseppe Di Guglielmo, Donovan Sproule, Nhan Tran, Russell Marroquin, Elham E Khoda, Vladimir Loncar, Audrey C Therrien, Jason Weitz, Dennis Plotnikov, Dmitri Demler, Javier Duarte, Keegan A Smith, Mohammad Mehdi Rahimifar, Hamza Ezzaoui Rahali, Karla Tame-Narvaez, *wa-hls4ml: A Benchmark and Surrogate Models for hls4ml Resource and Latency Estimation*, ACM Transactions on Reconfigurable Technology and Systems, Vol. 19, No. 2, 2026, pp. 1-29, h-index 38
- J28. Joseph Zuckerman, Martin Cochet, Maico Cassel Dos Santos, Erik Jens Loscalzo, Karthik Swaminathan, Tianyu Jia, Davide Giri, Thierry Tambe, Jeff Jun Zhang, Alper Buyuktosunoglu, Kuan-Lin Chiu, Giuseppe Di Guglielmo, Paolo Mantovani, Luca Piccolboni, Gabriele Tombesi, David Trilla, John-David Wellman, En-Yu Yang, Aporva Amarnath, Ying Jing, Bakshree Mishra, Joshua Park, Vignesh Suresh, Samira Zaliasl, Michael Lekas, Stephen Cahill, Hesam Sadeghi, Joseph Meyer, Noah Sturcken, Sarita Adve, David Brooks, Gu-Yeon Wei, Kenneth L Shepard, Pradip Bose, Luca P Carloni, *EPOCHS-1: A 12 nm Highly Heterogeneous Open-Source SoC With Distributed Coin-Based Power Management and Integrated Hybrid Voltage Regulation*, IEEE Journal of Solid-State Circuits, September 2025, h-index 243
- J27. ✿ Madhav Narayan Bhat, Marco Russo, Luca P. Carloni, Giuseppe Di Guglielmo, Farah Fahim, Andy C.Y. Li, Gabriel N. Perdue, *Machine learning for arbitrary single-qubit rotations on an embedded device*, Springer Nature: Quantum Machine Intelligence, Vol. 7, No. 1, June 2025, h-index 23
- J26. ✿ M. Aamir et al., *Using graph neural networks to reconstruct charged pion showers in the CMS High Granularity Calorimeter*, Journal of Instrumentation (JINST), Vol. 19, No. 11, November 2024, P11025, h-index 69
- J25. ✿ Jieun Yoo, Jennet Dickinson, Morris Swartz, Giuseppe Di Guglielmo, Alice Bean, Douglas Berry, Manuel Blanco Valentin, Karri DiPetrillo, Farah Fahim, Lindsey Gray, James Hirschauer, Shruti R Kulkarni, Ron Lipton, Petar Maksimovic, Corrinne Mills, Mark S Neubauer, Benjamin Parpillon, Gauri Pradhan, Chinara Syal, Nhan Tran, Dahai Wen, Aaron Young, *Smart pixel sensors: towards on-sensor filtering of pixel clusters with deep learning*, Machine Learning: Science and Technology, Vol. 5, No. 3, August 2024, h-index 41
- J24. ✿ Bernardita Štitić, Luca Urbinati, Giuseppe Di Guglielmo, Luca P Carloni, Mario R Casu, *Enhanced Machine-Learning Flow for Microwave-Sensing Systems for Contaminant Detection in Food*, IEEE Transactions on AgriFood Electronics, Vol. 2, No. 2, September 2024
- J23. ✿ Yumou Wei, Ryan F Forelli, Chris Hansen, Jeffrey P Levesque, Nhan Tran, Joshua C Agar, Giuseppe Di Guglielmo, Michael E Mauel, Gerald A Navratil, *Low latency optical-based mode tracking with machine learning deployed on FPGAs on a tokamak*, AIP Publishing: Review of Scientific Instruments, Vol. 95, No. 7, July 2024
- J22. ✿ Manuel B. Valentin, Giuseppe Di Guglielmo, Danny Noonan, Priyanka Dilip, Panpan Huang, Adam Quinn, Thomas Zimmerman, Davide Braga, Seda Ogrenci, Chris Jacobsen, Nhan Tran, Farah Fahim,

In-pixel AI for lossy data compression at source for X-ray detectors, Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, Vol. 1057, December 2023, h-index 187

- J21.  Allison McCarn Deiana, Nhan Tran, Joshua Agar, Michaela Blott, Giuseppe Di Guglielmo, Javier Duarte, Philip Harris, Scott Hauck, Mia Liu, Mark S Neubauer, Jennifer Ngadiuba, Seda Ogrenci-Memik, Maurizio Pierini, Thea Aarrestad, Steffen Bahr, Jurgen Becker, Anne-Sophie Berthold, Richard J Bonventre, Tomas E Muller Bravo, Markus Diefenthaler, Zhen Dong, Nick Fritzsche, Amir Gholami, Ekaterina Govorkova, Kyle J Hazelwood, Christian Herwig, Babar Khan, Sehoon Kim, Thomas Klijsma, Yaling Liu, Kin Ho Lo, Tri Nguyen, Gianantonio Pezzullo, Seyedramin Rasoulinezhad, Ryan A Rivera, Kate Scholberg, Justin Selig, Sougata Sen, Dmitri Strukov, William Tang, Savannah Thais, Kai Lukas Unger, Ricardo Vilalta, Belina von Krosigk, Thomas K Warburton, Maria Acosta Flechas, Anthony Aportela, Thomas Calvet, Leonardo Cristella, Daniel Diaz, Caterina Doglioni, Maria Domenica Galati, Elham E Khoda, Farah Fahim, Davide Giri, Benjamin Hawks, Duc Hoang, Burt Holzman, Shih-Chieh Hsu, Sergo Jindariani, Iris Johnson, Raghav Kansal, Ryan Kastner, Erik Katsavounidis, Jeffrey Krupa, Pan Li, Sandeep Madireddy, Ethan Marx, Patrick McCormack, Andres Meza, Jovan Mitrevski, Mohammed Attia Mohammed, Farouk Mokhtar, Eric Moreno, Srishti Nagu, Rohin Narayan, Noah Palladino, Zhiqiang Que, Sang Eon Park, Subramanian Ramamoorthy, Dylan Rankin, Simon Rothman, Ashish Sharma, Sioni Summers, Pietro Vischia, Jean-Roch Vlimant, Olivia Weng, *Applications and Techniques for Fast Machine Learning in Science*, Frontiers in Big Data, Vol. 5, 2022, h-index 10
- J20. Yeon-jae Jwa, Giuseppe Di Guglielmo, Lukas Arnold, Luca Carloni, Georgia Karagiorgi, *Real-time Inference with 2D Convolutional Neural Networks on Field Programmable Gate Arrays for High-rate Particle Imaging Detectors*, Frontiers in Artificial Intelligence, Vol. 5, 2022, h-index 47
- J19. Thea Aarrestad, Vladimir Loncar, Maurizio Pierini, Sioni Summers, Jennifer Ngadiuba, Christoffer Petersson, Hampus Linander, Yutaro Iiyama, Giuseppe Di Guglielmo, Javier Duarte, Philip Harris, Dylan Rankin, Sergo Jindariani, Kevin Pedro, Nhan Tran, Mia Liu, Edward Kreinar, Zhenbin Wu, and Duc Hoang, *Fast convolutional neural networks on FPGAs with hls4ml*, Machine Learning: Science and Technology, Vol. 2, No. 4, 2021, h-index 14
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- U8. 🌟 Flor Sanders, Gaurav Agarwal, Luca Carloni, Giuseppe Di Guglielmo, Andy C.Y. Li, Gabriel N. Perdue, *Fast Machine Learning for Quantum Control of Microwave Qudits on Edge Hardware*, June 2025, arXiv:2506.03323
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- U6.  Jennet Dickinson, Rachel Kovach-Fuentes, Lindsey Gray, Morris Swartz, Giuseppe Di Guglielmo, Alice Bean, Doug Berry, Manuel Blanco Valentin, Karri DiPetrillo, Farah Fahim, James Hirschauer, Shruti R Kulkarni, Ron Lipton, Petar Maksimovic, Corrinne Mills, Mark S Neubauer, Benjamin Parpillon, Gauri Pradhan, Chinar Syal, Nhan Tran, Dahai Wen, Jieun Yoo, Aaron Young, *Smartpixels: Towards on-sensor inference of charged particle track parameters and uncertainties*, December 2023, arXiv:2312.11676
- U5.  David Xu, A. Barış Özgüler, Giuseppe Di Guglielmo, Nhan Tran, Gabriel N Perdue, Luca Carloni, and Farah Fahim, *Neural network accelerator for quantum control*, August 2022, arXiv:2208.02645
- U4.  Hendrik Borras, Giuseppe Di Guglielmo, Javier Duarte, Nicolò Ghielmetti, Ben Hawks, Scott Hauck, Shih-Chieh Hsu, Ryan Kastner, Jason Liang, Andres Meza, Jules Muhizi, Tai Nguyen, Rushil Roy, Nhan Tran, Yaman Umuroglu, Olivia Weng, Aidan Yokuda, Michaela Blott, *Open-source FPGA-ML codesign for the MLPerf Tiny Benchmark*, June 2022, arXiv:2206.11791
- U3. Luca Piccolboni, Giuseppe Di Guglielmo, and Luca P. Carloni, *Securing accelerators with dynamic information flow tracking*, IEEE International Symposium on Hardware Oriented Security and Trust (HOST), Washington, DC, USA, May 6-10, 2019, pp. 1-2
- U2. Paolo Mantovani, Emilio G. Cota, Seongjong Kim, Kevin Tien, Johnnie Chan, Giuseppe Di Guglielmo, Christian Pilato, Martha A. Kim, Mingoo Seok, Kenneth Shepard, and Luca P. Carloni, *Benchmarking methodology for embedded scalable platforms*, SEAK Workshop, San Francisco, CA, USA, June 1, 2014
- U1. Giuseppe Di Guglielmo, Masahiro Fujita, Franco Fummi, Graziano Pravadelli, Stefano Soffia, *EFSM-based Weight-oriented Concolic Testing for Embedded Software*, IEICE Technical Report, Vol. 110, No. 316, pp. 19-24, November 11, 2010

Tutorials

- T9.  *Even Higher-Level Synthesis: An Exploration of AI Hardware Accelerators Using hls4ml*, ACM/IEEE Design Automation Conference (DAC), June 22-25, 2025
- T8. *ESP: the Open-Source Research Platform for Agile SoC Design and Programming*, ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), 2021
- T7. *ESP: an Open-Source Platform for Agile SoC Development*, IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), 2021
- T6. *ESP: an Open-Source Platform for Agile SoC Development*, IEEE/ACM International Symposium on Microarchitecture (MICRO), 2020
- T5. *ESP: an Open-Source Platform for Interdisciplinary Research on SoC Design and Programming*, International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), 2020
- T4. *Open-Source Hardware: Heterogeneous System Integration with Embedded Scalable Platforms*, Embedded Systems Week (ESWEEK), October 13-18, 2019
- T3. *Assertion based verification: a common verification infrastructure for SoC and embedded software*, ACM/IEEE Design, Automation and Test in Europe (DATE), March 18-22, 2013
- T2. *Assertion-based verification for SoC and embedded software*, ACM/IEEE/IEICE Asia and South Pacific Design Automation Conference (ASP-DAC), January 30 - February 2, 2012
- T1. *Verifying reliability*, Dagstuhl Seminar 12341, Germany, August 18-24, 2012

Awards

- A6. 🏆 Best student paper award for “Enhanced Machine-Learning Flow for Microwave-Sensing Systems to Detect Contaminants in Food”, IEEE Conference on AgriFood Electronics (CAFE), 2023
- A5. Best paper finalist for “ESP4ML: Platform-Based Design of Systems-on-Chip for Embedded Machine Learning”, ACM/IEEE Conference on Design, Automation and Test in Europe (DATE), 2020
- A4. Best Session Presentation Award for “Automatic Revisioning of Communication Interfaces for Compositional High-Level Synthesis of SoCs”, Semiconductor Research Corporation TECHON, 2014
- A3. Best paper finalist for “Dynamic property mining for embedded software”, IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis, 2012
- A2. Best paper finalist for “FATE: A Functional ATPG to Traverse Unstabilized EFSMs”, IEEE European Test Symposium, 2006
- A1. First prize winner of competition “Applicazioni per Terminali Mobili”, 2004, Telecom Italia Lab (TiLab), Torino, Italy

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